CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of producing a thin, high-quality, substantially relaxed SiGe-on-insulator substrate material comprising the steps of:

(a) forming a SiGe or pure Ge layer on a surface of a first single crystal Si layer, said first single crystal Si layer is present atop a barrier layer that is resistant to Ge diffusion; and

(b) heating said layers at a temperature which permits interdiffusion of Ge throughout said first single crystal Si layer and said SiGe or pure Ge layer thereby forming a substantially relaxed, single crystal SiGe layer atop said barrier layer.

2. The method of Claim 1 wherein said first single crystal Si layer and said barrier layer are components of a silicon-on-insulator (SOI) substrate.

3. The method of Claim 1 wherein said first single crystal Si layer and said barrier layer are components of a non-SOI substrate.

4. The method of Claim 3 wherein said first single crystal Si layer has a thickness of from about 1 to about 2000 nm.

5. The method of Claim 1 wherein said barrier layer is a patterned barrier layer.

6. The method of Claim 1 wherein said barrier layer is an unpatterned barrier layer.

7. The method of Claim 1 wherein said barrier layer comprises crystalline or non-crystalline oxides, or crystalline or non-crystalline nitrides.

8. The method of Claim 1 wherein said barrier layer is a buried oxide region that is patterned or unpatterned.

9. The method of Claim 1 wherein said barrier layer has a thickness of from about 1 to about 1000 nm.

10. The method of Claim 1 wherein a SiGe layer comprising up to 99.99 atomic percent Ge is employed in step (a).

11. The method of Claim 10 wherein said SiGe layer comprises from about 10 to about 35 atomic percent Ge.

12. The method of Claim 1 wherein said SiGe or pure Ge layer is formed by an epitaxial growth process selected from the group consisting of low-pressure chemical vapor deposition, atmospheric pressure chemical vapor deposition, ultra-high vacuum chemical vapor deposition, molecular beam epitaxy, and plasma-enhanced chemical vapor deposition.

13. The method of Claim 1 wherein a pure Ge layer is employed in step (a).

14. The method of Claim 1 further comprising forming a Si cap layer atop said SiGe or pure Ge layer prior to performing step (b).

15. The method of Claim 14 wherein said Si cap layer comprises epi-Si, a:Si, single or polycrystalline Si or any combination and multilayer thereof.

16. The method of Claim 15 wherein said Si cap layer comprises epi-Si.

17. The method of Claim 14 wherein said Si cap layer has a thickness of from about 1 to about 100 nm.

18. The method of Claim 1 wherein a surface oxide layer forms during said heating step.

19. The method of Claim 18 wherein said surface oxide layer has a thickness of from about 10 to about 1000 nm.

20. The method of Claim 18 further comprising removing said surface oxide layer utilizing a wet chemical etch process.

21. The method of Claim 1 wherein steps (a)-(b) are repeated any number of times.

22. The method of Claim 1 wherein said heating step is carried out in an oxidizing ambient which comprises at least one oxygen-containing gas.

23. The method of Claim 22 wherein said at least one oxygen-containing gas comprises O_2, NO, N_2O, ozone, air or mixtures thereof.

24. The method of Claim 22 further comprising an inert gas, said inert gas being employed to dilute said at least one oxygen-containing gas.

25. The method of Claim 1 wherein said heating step is performed at a temperature of from about 900° to about 1350°C.

26. The method of Claim 25 wherein said heating step is performed at a temperature of from about 1200° to about 1335°C.

27. The method of Claim 1 wherein said substantially relaxed SiGe layer has a thickness of about 2000 nm or less.

28. The method of Claim 27 wherein said substantially relaxed SiGe layer has a thickness of from about 10 to about 100 nm.

29. The method of Claim 1 wherein said substantially relaxed SiGe layer has a defect density of less than about 10^8 defects/cm^2.

30. The method of Claim 1 wherein said substantially relaxed SiGe layer has a measured lattice relaxation of from about 1 to about 100 %.

31. The method of Claim 30 wherein said substantially relaxed SiGe layer has a measured lattice relaxation of from about 50 to about 80 %.

32. The method of Claim 1 further comprising growing an additional SiGe layer atop said substantially relaxed SiGe layer.

33. The method of Claim 32 further comprising forming a strained Si layer atop said additional SiGe layer.

34. The method of Claim 1 further comprising forming a strained Si layer atop said substantially relaxed SiGe layer.

35. A substrate material comprising:

a Si-containing substrate;

an insulating region that is resistant to Ge diffusion present atop said Si-containing substrate; and

a substantially relaxed SiGe layer present atop said insulating region, wherein said substantially relaxed SiGe layer has a thickness of about 2000 nm or less.

36. The substrate material of Claim 35 wherein said insulating region is patterned.

37. The substrate material of Claim 35 wherein said insulating region is unpatterned.

38. The substrate material of Claim 35 wherein said insulating region comprises crystalline or non-crystalline oxides, or crystalline or non-crystalline nitrides.

39. The substrate material of Claim 35 wherein said insulating region is a buried oxide region that is patterned or unpatterned.

40. The substrate material of Claim 35 wherein said insulating region has a thickness of from about 1 to about 1000 nm.

41. The substrate material of Claim 35 wherein said substantially relaxed SiGe layer has a thickness of from about 10 to about 100 nm.

42. The substrate material of Claim 36 wherein said substantially relaxed SiGe layer has a measured lattice relaxation of from about 1 to about 100 %.

43. The substrate material of Claim 42 wherein said substantially relaxed SiGe layer has a measured lattice relaxation of from about 50 to about 80 %.

44. A heterostructure comprising:

a Si-containing substrate;

an insulating region that is resistant to Ge diffusion present atop the Si-containing substrate;

a substantially relaxed SiGe layer present atop the insulating region, wherein the substantially relaxed SiGe layer has a thickness of about 2000 nm or less;

and a strained Si layer formed atop the substantially relaxed SiGe layer.

45. The heterostructure of Claim 44 wherein said insulating region is patterned.

46. The heterostructure of Claim 44 wherein said insulating region is unpatterned.

47. The heterostructure of Claim 44 wherein said insulating region comprises crystalline or non-crystalline oxides, or crystalline or non-crystalline nitride.

48. The heterostructure of Claim 44 wherein said insulating region barrier layer is a buried oxide region that is patterned or unpatterned.

49. The heterostructure of Claim 44 wherein said insulating region has a thickness of from about 20 to about 200 nm.

50. The heterostructure of Claim 44 wherein said substantially relaxed SiGe layer has a thickness of from about 10 to about 100 nm.

51. The heterostructure of Claim 44 wherein said substantially relaxed SiGe layer has a measured lattice relaxation of from about 1 to about 100 %.

52. The heterostructure of Claim 51 wherein said substantially relaxed SiGe layer has a measured lattice relaxation of from about 50 to about 80 %.

53. The heterostructure of Claim 44 wherein said strained Si layer has a thickness of from about 1 to about 100 nm.

54. The heterostructure of Claim 44 wherein said strained Si layer comprises an epi-Si layer.

55. The heterostructure of Claim 44 wherein alternating layers of relaxed SiGe and strained Si are formed atop said strained Si layer.

56. The heterostructure of Claim 44 wherein said strained Si layer is replaced with a lattice mismatched compound selected from the group consisting of GaAs and GaP.